

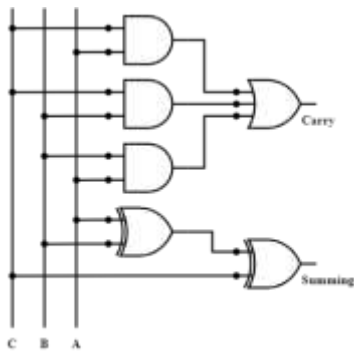
1-BIT Full Adder Virtual Trainer For Electrical Engineering Education

Miftah Muhammad, Dharmawan*, Suparman

Department of Electrical Engineering, Faculty of Engineering, Khairun University.

*Corresponding author
dharmawan@unkhair.ac.id

Graphical Abstract



Abstract

The increasing complexity of digital logic design and the rapid evolution of remote learning environments have highlighted the need for innovative educational tools in electrical engineering. Traditional laboratory-based methods, while effective for hands-on learning, often face challenges related to cost, accessibility, and infrastructure limitations, which restrict student engagement and practice opportunities. In response, this study presents the development of a 1-bit Full Adder Virtual Trainer designed to enhance conceptual understanding and practical skill acquisition in digital logic courses. The system integrates interactive simulation, real-time logic evaluation, and visual feedback to facilitate comprehension of fundamental circuit behavior. Evaluation results indicate that the trainer effectively improves students' understanding of logic operations and circuit functionality through direct experimentation with input variables. The tool also serves as a viable substitute for physical laboratory equipment, providing an accessible, efficient, and scalable solution for institutions with limited resources. Overall, the proposed virtual trainer strengthens the connection between theory and practice, supporting flexible and inclusive learning in electrical engineering education.

Keywords: Virtual Trainer, Full Adder, Digital Logic, Electrical Engineering Education, Interactive Learning



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1. INTRODUCTION

The necessity for innovative educational tools in electrical engineering, particularly in digital logic design, has become increasingly apparent given the complexities of the subject matter and the evolving landscape of remote learning [1]. The recent global shift towards hybrid learning models, exacerbated by events like the COVID-19 pandemic, further underscores the demand for effective virtual platforms that can bridge the gap between theoretical knowledge and practical application [2] [3]. To address this, the integration of virtual reality and gamification techniques offers a promising avenue for creating engaging and interactive learning experiences in digital electronics [4]. Traditional laboratory settings, while invaluable for hands-on experience, often present challenges related to cost, infrastructure, and accessibility, making virtual laboratories a compelling, cost-effective alternative for practical skill development [5] [6].

Despite the recognized importance of laboratory-based learning, many educational institutions still face limitations in providing sufficient access to physical trainer kits and laboratory sessions, particularly for large classes or remote learners. This lack of access can hinder students' understanding of how digital circuits function in real time, especially for foundational topics such as combinational logic and arithmetic circuits. Furthermore, conventional methods often lack interactive visualization tools that can effectively demonstrate the dynamic behavior of logical operations, which is crucial for deeper conceptual understanding [7]. This situation creates a significant gap between theoretical instruction and practical experimentation, particularly in courses involving basic circuit design and logic system implementation [3].

To overcome these challenges, virtual trainers have emerged as a viable and scalable solution that combines visual learning, interactivity, and simulation-based experimentation. Such platforms allow students to

manipulate input variables, observe circuit behavior, and immediately visualize the resulting outputs, thereby reinforcing the cause–effect relationship in logic operations. Virtual learning environments can also simulate complex systems and scenarios that might be impractical or unsafe to replicate in a physical lab, offering a safe space for experimentation and error correction [8]. Moreover, virtual and remote lab platforms, specifically designed for electronics, have been developed as low-cost alternatives to traditional setups, providing students with accessible tools for hands-on learning even from a distance [9]. These systems often integrate electronic simulators, quizzes, and assessment modules to help learners test their understanding of logic gates and combinatorial circuits in an engaging and interactive manner [10].

While previous studies have successfully introduced virtual laboratory systems for electronics and logic circuit simulation, most of these efforts focus on general-purpose simulation environments or complex circuit analysis tools, which may not adequately support beginner-level learning of fundamental digital concepts. As a result, there remains a clear research gap in developing specialized virtual trainers that specifically target basic building blocks of digital logic design—such as the 1-bit full adder—through simplified, interactive, and visually guided learning environments. Addressing this gap is essential to ensure that students not only understand theoretical logic principles but can also relate them to real-time circuit operations.

Building upon this foundation, this study presents the development of a 1-bit Full Adder Virtual Trainer aimed at enhancing conceptual understanding and practical skills in digital logic education. The proposed trainer integrates interactive input control, real-time logic evaluation, and visual feedback to help students dynamically explore logic relationships and circuit behavior. By enabling experimentation without physical hardware constraints, the trainer provides an accessible and cost-effective solution for institutions with limited laboratory resources. Supported by previous evidence on the effectiveness of virtual and gamified learning systems in improving engagement and comprehension [11]–[15], the objective of this research is to design and implement a 1-bit Full Adder Virtual Trainer that functions as a low-cost, interactive substitute for physical trainer kits, thereby strengthening the link between theory and practice in digital electronics education.

2. METHOD

This study employs a developmental research approach focused on designing and constructing a 1-bit Full Adder Virtual Trainer as an innovative digital learning tool for electrical engineering students. The research followed a structured development process consisting of four main stages: planning and requirement analysis, system design, implementation, and testing and evaluation.

At Planning and Requirement Analysis sections, the functional and educational requirements of the virtual trainer were identified. The main objective was to design a learning tool that enables students to visualize, interact with, and understand the logic operations of a 1-bit full adder without relying on physical trainer kits. Reference materials from digital logic design theory and previous virtual learning systems were analyzed to determine the key features to be included, such as real-time simulation, input control, and visual feedback of logic operations.

The system was designed to simulate the operation of a 1-bit full adder circuit, which produces two outputs Sum (Σ) and Carry (Cout) based on three binary inputs (A, B, and C). The logical relationships are defined as follows:

1. Σ | *summing* = $(A \oplus B) \oplus C$
2. $\cup$ | *Carry* = $(A.B) + (B.C) + (A.C)$

Where:

- $\oplus$ denotes the XOR (exclusive OR) logic operation
- $.$ denotes the AND operation
- $+$ denotes the OR operation

These equations were embedded directly into the virtual trainer's algorithm to reproduce the logical process of a 1-bit full adder. The circuit schematic used as a reference for the digital simulation is shown in Figure 1, and its corresponding truth table is presented in Table 1.

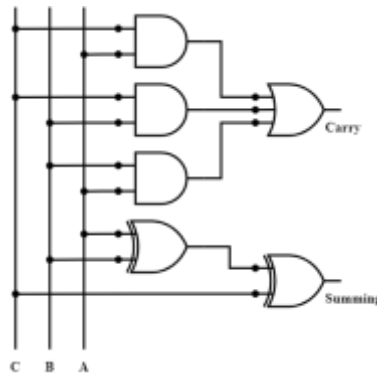


Figure 1. 1-Bit Full Adder Schematic

Table 1. 1-bit full adder truth table

C	B	A	Σ	U
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The virtual trainer was implemented using a graphical user interface (GUI) that allows users to manipulate inputs (A, B, C) and observe real-time changes in Sum and Carry outputs. The interface was designed to be intuitive and accessible, enabling users to understand how different combinations of binary inputs affect the circuit's outputs. Visual indicators and color-coded logic states were integrated to enhance interactivity and engagement.

After development, the system underwent functionality testing to ensure accurate logical operations according to the 1-bit full adder truth table. The evaluation focused on verifying the correctness of the simulation, responsiveness of the interface, and reliability of the logic computation. Informal usability feedback was collected from students to assess clarity, ease of use, and perceived learning benefits.

Through these stages, the development process produced a functional virtual simulation tool that dynamically represents the binary addition process. The real-time interaction allows students to observe how logic gates (XOR, AND, OR) work together to generate outputs, fostering a clearer conceptual understanding of digital circuits. This developmental approach demonstrates how virtual environments can effectively serve as practical substitutes for physical trainers, improving both conceptual learning and hands-on experience in digital electronics education.

3. RESULTS AND DISCUSSION

The final output of the development process was a 1-bit Full Adder Virtual Trainer built as a portable executable (.exe) application using VB.NET. The system successfully simulated binary addition processes according to the Boolean logic equations of a full adder circuit, providing two output states Sum (Σ) and Carry (Cout) in real time. The design incorporated interactive controls and logic visualization features to enhance student engagement and comprehension.

Functional testing was carried out to verify that the virtual trainer correctly implemented all logic combinations of the full adder truth table. Using systematic input testing across the eight possible input combinations (A, B, and C), the system achieved a 100% accuracy rate in generating the correct output pairs (Σ and Cout). The average response time for logic updates after input toggling was measured at less than 100 milliseconds, ensuring smooth real-time performance without noticeable delay. These results confirm that the virtual simulation accurately replicates the expected logical behavior of a hardware full adder circuit.

The usability aspect of the 1-bit Full Adder Virtual Trainer was analyzed based on key design principles in human-computer interaction, including ease of use, clarity, functionality, and accessibility. The application was

developed as a portable executable (.exe) program that can run directly without installation, ensuring high compatibility and minimal system dependency. This design decision enhances usability by allowing both instructors and students to operate the trainer on any Windows-based computer with minimal technical preparation.

From a pedagogical standpoint, the virtual trainer was conceived as a substitute for the absence of physical hardware trainers commonly used in introductory microprocessor laboratories. Limited access to such hardware often restricts students' opportunities to engage in practical experimentation. By providing a virtual simulation environment, the system replicates the logic behavior of a real full adder circuit, enabling users to manipulate binary inputs and observe corresponding Sum and Carry outputs in real time. This functionality effectively supports the same learning objectives as hardware-based experiments, but with greater flexibility and accessibility.

The application interface was designed to be intuitive and visually clear, with three toggle buttons (A, B, and C) representing input variables and LED-style indicators displaying the output logic states. The use of color-coded visual feedback (red for logic "1," gray for logic "0") and dynamic Boolean expression updates reinforces user comprehension of logical processes. These design choices align with established usability principles that emphasize immediate system feedback and visual mapping, allowing users to quickly interpret system responses and understand logic flow. The 1-Bit Full Adder Virtual Trainer design can be seen in figure 2

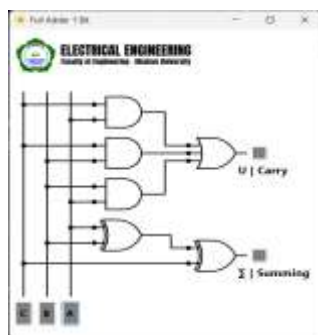


Figure 2. 1-Bit Full Adder Virtual Trainer Display

In summary, the preliminary usability analysis indicates that the virtual trainer meets essential criteria for a user-friendly educational tool. It offers a practical and scalable alternative for institutions facing constraints in laboratory infrastructure, enabling continuous and interactive learning experiences even without access to physical trainer kits. By translating abstract Boolean logic into an accessible visual format, the system successfully supports fundamental learning outcomes in digital electronics and microprocessor education. The 1-Bit Full Adder output display can be seen in Table 2.

Table 2. 1-bit full adder output indicator display

C	B	A	Σ	U
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	1
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

4. CONCLUSION

This study successfully developed a 1-bit Full Adder Virtual Trainer as an interactive and accessible educational tool for digital logic learning in electrical engineering. The system effectively simulates the logical behavior of a full adder circuit, enabling users to perform and observe binary addition processes dynamically without the need for physical hardware. The integration of real-time logic evaluation, visual indicators, and

Boolean expression visualization demonstrates how virtual tools can support both conceptual understanding and practical skill acquisition in foundational digital electronics learning.

The results indicate that the trainer operates with high logical accuracy and efficient system performance, while the preliminary usability analysis confirms that its interface design meets essential usability criteria such as clarity, interactivity, and ease of access. More importantly, the virtual trainer serves as a functional substitute for unavailable laboratory hardware, offering a flexible and cost-effective solution for institutions with limited practical infrastructure. This aligns with the growing need for digital learning tools that can bridge the gap between theoretical instruction and hands-on experimentation in modern engineering education.

However, several limitations were identified. The current version is restricted to 1-bit adder operations and remains platform-dependent, functioning only on Windows environments. The interface design, although effective for basic logic visualization, lacks scalability for more complex circuits or collaborative multi-user scenarios. Future development should therefore focus on expanding the system's functionality to include multi-bit operations, additional arithmetic modules such as subtractors or ALUs, and web-based deployment to support remote and cooperative learning environments.

In conclusion, the developed 1-bit Full Adder Virtual Trainer demonstrates the potential of simulation-based tools as a viable and pedagogically valuable alternative to traditional hardware-based laboratories, particularly in contexts where accessibility and cost are significant constraints. It reinforces the critical role of interactive visualization in strengthening the connection between theoretical learning and practical understanding within digital logic education.

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